FPGA VARIABLE BASE CHIRP PULSE GENERATOR FOR SYNTHETIC APERTURE RADAR ONBOARD UNMANNED AERIAL VEHICLE SYSTEM

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ABSTRACT

Synthetic Aperture Radar (SAR) is one of active microwave sensor could work all weather and day/night time. This system can observe the objects on ground surface, and obtain microwave image by SAR image processing. SAR needs modulated signal like chirp pulse for high resolution and preciseness. In the case of UAV, some pulse parameter, i.e. bandwidth etc, should be changed to adequate value during flight or mission for stable platform posture. This paper discusses the proposed FPGA variable based chirp pulse generator to solve the platform posture effect on our UAV SAR mission.

Keywords: SAR, UAV, FPGA, Chirp pulse

INTRODUCTION

Microwave Remote Sensing is effective method to observe and analyze the earth deformation. We are developing Circularly Polarized Synthetic Aperture Radar(CP-SAR) system, sensor and platform. Two kind of observation platforms, Unmanned Aerial Vehicle(UAV) and small satellite are considered in our project. UAV SAR system is our first mission in research project. The benefit of UAV remote sensing is ease of scramble and configurable comparing with satellite. Pulse specification of SAR system must be configured to match platform and observation situation. In the case of UAV SAR system, many observation condition is very unstable, means that it's always changing during observation. One of variable condition is platform condition, like a UAV flight speed, flight angle(pitch, yaw, and roll ), altitude. Another one of variable condition is environmental factor, like a weather, wind speed and wind direction. In this situation, the most ideal pulse specification is also frequently changing. So automatical variability of pulse specification is required to get more precise SAR image. According with this opinion, we develop chirp signal generator with standalone pulse calculator by using FPGA and PC. This research is still prototype of our required SAR system. In future, we will transfer some functions of PC into FPGA, and complete SAR system consist of only FPGA and Telecommunication devices.

MATERIALS AND METHODS / EXPERIMENTAL

Basic architecture of our SAR transceiver system is shown Figure 1.
SAR transmitter mainly consists of RF transceiver, FPGA development board with DAC daughter card and onboard PC. Chirp signal generator and pulse calculator are embedded in FPGA. These hardware modules are designed by HDL, and run without on-chip CPU and software program because these modules must be high speed processing. Chirp signal generator is signal generator to output chirp signal, modulated sine wave signal with linear frequency change on time domain used for observation pulse. This signal is expressed as equation (1).

\[
St(i) = \exp\left(i \frac{\pi B t^2}{\tau}\right) \quad (1)
\]

\( B \) means bandwidth or frequency change width, frequency change width. \( \tau \) is pulse time duration. Chirp signal consists of two channel, I-ch(In-phase channel, means real value expressed by cosine) and Q-ch(Quadrature channel, means imaginary value expressed by sine). Function of chirp signal generator is output of both two signal, I-ch and Q-ch. These two signal is combined to one complex chirp signal after converted to L-band analog signal in RF transceiver device. Chirp signal generator works by DDS(Direct Digital Synthesizer) method. DDS method is one way to get signal value by unit circle phase information related with sine wave amplitude value. Simple theory of DDS method is shown as figure 2.

Figure 2. Theory of DDS method

Unit circle phase is divided many parts. For example, in the case of normal sine wave, the current phase shift these parts one by one, and if this phase shift through whole circle is finish in just one second, sine wave frequency is 1Hz. So phase information means distance of phase shift and it called as Tuning word. DDS method can output many kind signal, like a saw tooth wave signal, triangle wave signal, square wave signal and of course chirp signal, by controlling phase shift. Tuning word for chirp signal is expressed as array because its phase shift is not linear while a pulse. This Tuning word array is calculated as equation(2).

\[
M(t) = \text{rect}\left(\frac{t}{\tau}\right) \cdot 2^n \frac{B}{f_s} \cdot t \left[\frac{\tau}{2}, \frac{\tau}{2}\right] \quad (2)
\]

The value of sampling frequency\( f_s \), chirp bandwidth \( B \), pulse time duration \( \tau \) and signal quantization bit-rate \( q \) is used as variable. Next, detailed hardware architecture of chirp signal generator is shown as figure 3.

Figure 3. Hardware architecture of chirp signal generator
Chirp signal generator consists of FPGA development board components and HDL designs, in particular on-board oscillator, phase lock loop, timing controller, phase accumulator, pulse calculator and DAC. On-board oscillator outputs base clock, phase Lock Loop converts clock from oscillator to required frequency clock as same as sampling frequency of DAC. Timing controller manages PRF, means that it sends pulse output enable to phase accumulator. Phase accumulator generates chirp signal and output it when the pulse output enable receive from timing controller. DAC converts digital chirp signal to analog chirp signal. This architecture needs two prepared data, tuning word LUT (array) and sine wave amplitude value array corresponding divided phase part to generate required chirp signal. We modified these LUT data more smaller to cut off usage memory resource and register word length, on purpose to decline signal time delay, power consumption and the amount of data to be rewritten more quickly (see Figure 4). Tuning word is needed only half of it, and sine wave amplitude is needed only quarter of it to express its whole data. Figure 5 shows work flow of chirp signal generator. Chirp signal generator has two state, wait(non-output) and active(output). In wait state, timing controller counts time interval until time elapse reaches Pulse Repetitive Interval(PRI). When counting is finished, state of chirp signal generator switches wait to active, starts to output chirp signal. In active state, work flow is more divided for five pipeline tasks. Pipeline1 is to calculate
tuning word LUT address. Pipeline 2 is to calculate tuning word value. Pipeline 3 is to calculate current unit circle phase. Pipeline 4 is to abbreviate unit circle phase for small sine amplitude LUT. Pipeline 5 is calculate output signal value. Purpose of this pipeline architecture is improvement of internal signal time delay. Pulse calculator is additional module of chirp signal generator to change output pulse specification. Function of this module is calculation of tuning word. Tuning word is calculated from bandwidth, sampling frequency and pulse duration as shown above section II. The order command includes bandwidth or pulse duration for tuning word. Pulse calculator receives order from outside device especially onboard PC, calculates and stores value, and adapt it from next interval or pulse. In pulse calculator, I use 32 bit fixed point format on purpose to meet both calculation speed and accuracy. Figure 6 shows calculation work flow. We assign actual number part initial 7 bits, and decimal fraction number part to last 25 bits. This format contain no sign part because all of value is always positive number. Pulse calculator work flow is also consists of some pipeline architecture as same as chirp signal generator. Almost all variable used in this work flow is integer format number, so digit shifting is only once in last process. Finally, result of calculation is 14 bits integer tuning word. This generated tuning word is used in chirp signal generator from next pulse output.

RESULTS AND DISCUSSION

We employed a DE2-115 FPGA development board distributed by Terasic for only development scene(Figure 7).

This development board equips Altera CycloneIV E(EP4CE115F29C7) FPGA. Figure 8 is statistics of signal time delay simulated by Altera TimeQuest Timing Analyzer. Maximum time delay is over 27 ns without pipeline architecture, but 5 pipelines improve the time delay around 2 ns.
8-a. No pipeline architecture  
8-b. 5 pipeline architecture

Figure 8. Statistics of FPGA internal signal time delay

9-a. Band width 30MHz, Pulse duration 0.5us, Sampling frequency 200MHz

9-b. Band width 50MHz, Pulse duration 2us, Sampling frequency 200MHz

9-c. Band width 100MHz, Pulse duration 4us, Sampling frequency 200MHz

Figure 9. Actual generated chirp signal and its frequency material
It is difficult to improve time delay any longer in architecture aspect. Therefore we suppose that more high speed grade FPGA is needed to solve this time delay problem completely. Figure 9 shows example of generated actual chirp signal and its frequency material. It shows that higher pulse duration will generate higher accuracy, because the number of sampling also increases, and to be enough amount to express detailed signal. We supposed that bandwidth is not important to gain high-level signal accuracy. In other words, lack of the number of sampling is the most troublesome and considerable. Making sampling frequency more higher is one of other solver but it is distant, because the signal delay problem is remain as a bottleneck. Decreasing bandwidth and increase pulse duration is actual solver but these solution cause decline of SAR image resolution. We could consider that pulse specification already has faced actual limit considering trade off between resolution and device cost. To solve this problem, we recommend to adapt low-pass filter module to generate chirp signal, this method is the simplest solution and fully effective.

CONCLUSION

This paper proposed FPGA variable based chirp pulse generator to solve the platform posture effect on our UAV SAR mission. The result shows that more pulse duration will generate higher accuracy, because the number of sampling also increases, and to be enough amount to express detailed signal. We supposed that bandwidth is not important to gain high-level signal accuracy. Even decreasing bandwidth and increase pulse duration is actual solver but these solution cause decline of SAR image resolution. To solve this problem, we recommended to adapt low-pass filter module to generate chirp signal, this method is the simplest solution and fully effective. In future research, our primary task is validation of chirp signal generator usability by real ground tests and UAV flight experiments. However, we will investigate the possibility of SAR processor onboard FPGA. Then we will blush up these modules and embed the SAR image processing function. In this time, we send orders by using slide switch and push button equipped in FPGA development board. We will replace this input method by USB or Ethernet connection from PC.

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